control bits 265 are distributed, as may be needed, to the various portions of the computation unit 200, such as the various input enables 251, input selects 252, output selects 253, MUX selects 254, DEMUX enables 256, DEMUX selects 257, and DEMUX output selects 258. The CU controller 255 also includes one or more lines 295 for reception of control (or configuration) information and transmission of status information.

On Page 29, starting on line 30, please replace the paragraph with the following:

Figure 9 is a block diagram illustrating, in greater detail, a preferred core cell 610 of an adaptive logic processor computational unit 600 with a fixed computational element 650, in accordance with the present invention. The fixed computational element is a 3-input–2 output function generator 550, separately illustrated in Figure 10. The preferred core cell 610 also includes control logic 655, control inputs 665, control outputs 670 (providing output interconnect), output 675, and inputs (with interconnect muxes) 660 (providing input interconnect).

IN THE CLAIMS:

Please amend the following claims, Claim 1, 4, 12, 13, 14, 15, 16, 35, 36, 40, 46, 52, 53, 55, 64, 74, 75, 90, 93, 99, 100, 102, 103, and 104 in accordance to the below changes. A marked up version of the changes, is attached hereto.

1. (Once Amended) A system for configuring and operating an adaptive circuit, the system comprising:

a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

a plurality of heterogeneous computational elements, a first computational element of the plurality of heterogeneous computational elements having a first fixed architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network capable of configuring and providing the first operand data to the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes in response to the first configuration information, and the interconnection network further capable of reconfiguring and providing the second operand data to the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes in response to the second configuration information, the first functional mode being different than the second functional mode.

4. (Once Amended) The system of claim 1, further comprising:

a memory coupled to the plurality of heterogeneous computational elements and to the interconnection network, the memory capable of storing the first configuration information and the second configuration information.

12. (Once Amended) The system of claim 1, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of specific architectures, the plurality of specific architectures comprising at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, routing, control, input, output, and field programmability.

13. (Once Amended) The system of claim 1, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

14. (Once Amended) The system of claim 1, further comprising:

a controller coupled to the plurality of heterogeneous computational elements and to the interconnection network, the controller capable of coordinating the configuration of the plurality of heterogeneous computational elements for the first functional mode with the first operand data and further coordinating the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode with the second operand data.

15. (Once Amended) The system of claim 1, further comprising:

a second plurality of heterogeneous computational elements coupled to the interconnection network, the second plurality of heterogeneous computational elements configured for a controller operating mode, the second plurality of heterogeneous computational elements capable of coordinating the configuration of the plurality of heterogeneous computational elements for the first functional mode with the first operand data and further coordinating the reconfiguration of the plurality of heterogeneous computational elements for the second functional mode with the second operand data.

16. (Once Amended) The system of claim 1, wherein the system is embodied within a mobile station having a plurality of operating modes, the plurality of operating modes comprising at least two of the following modes: a mobile telecommunication mode, a personal digital assistance mode, a multimedia reception mode, a mobile packet-based communication mode, and a paging mode.

35. (Once Amended) The module of claim 31, wherein the first information sequence and the second information sequence have a discrete packet form.

36. (Once Amended) The module of claim 31, wherein the first information sequence and the second information sequence have a continuous stream form.

40. (Once Amended) A method for adaptive configuration and operation, the method comprising:

receiving a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

in response to the first configuration information, configuring through an interconnection network and providing the first operand data to a plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes, a first computational element of the plurality of heterogeneous computational elements having a first fixed

architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture; and

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in response to the second configuration information, reconfiguring through the interconnection network and providing the second operand data to the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes, the first functional mode being different than the second functional mode.

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46. (Once Amended) The method of claim 40, further comprising:

storing the first configuration information as a configuration of the plurality of heterogeneous computational units.

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52. (Once Amended) The method of claim 40, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of specific architectures, the plurality of specific architectures comprising at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, routing, and field programmability.

53. (Once Amended) The method of claim 40, wherein the plurality of functional modes comprising at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

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55. (Once Amended) The method of claim 40, wherein the method is operable within a mobile station having a plurality of operating modes, the plurality of operating modes comprising at least two of the following modes: a mobile telecommunication mode, a personal digital assistance mode, a multimedia reception mode, a mobile packet-based communication mode, and a paging mode.

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64. (Once Amended) A method for adaptive configuration, the method comprising:

transmitting a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

wherein when a first executable information module is received, an interconnection network coupled to a plurality of heterogeneous computational elements is capable of configuring and providing the first operand data to the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes in response to the first configuration information, and the interconnection network further capable of reconfiguring and providing the second operand data to the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes in response to the second configuration information, the first functional mode being different than the second functional mode; and

wherein the plurality of heterogeneous computational elements include a first computational element and a second computational element, the first computational element having a first fixed architecture and the second computational element having a second fixed architecture, the first fixed architecture being different than the second fixed architecture.

74. (Once Amended) The method of claim 64, wherein the first fixed architecture and the second fixed architecture are selected from a plurality of specific architectures, the plurality of specific architectures comprising at least two of the following functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

75. (Once Amended) The method of claim 64, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations.

90. (Once Amended) The adaptive integrated circuit of claim 88, wherein the plurality of functional modes comprises at least two of the following functional modes: linear algorithmic

operations, non-linear algorithmic operations, finite state machine operations, controller operations, memory operations, and bit-level manipulations.

93. (Once Amended) The adaptive integrated circuit of claim 88, wherein the plurality of fixed and differing computational elements are selected from a plurality of specific architectures, the plurality of specific architectures comprising at least two of the following corresponding functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability.

99. (Once Amended) An adaptive integrated circuit, comprising:

a plurality of executable information modules, a first executable information module of the plurality of executable information modules and a second executable information module of the plurality of executable information modules each having corresponding operand data;

a plurality of reconfigurable matrices, the plurality of reconfigurable matrices including a plurality of heterogeneous computation units, each heterogeneous computation unit of the plurality of heterogeneous computation units formed from a selected configuration, of a plurality of configurations, of a plurality of fixed computational elements, the plurality of fixed computational elements including a first computational element having a first architecture and a second computational element having a second architecture, the first architecture distinct from the second architecture, the plurality of heterogeneous computation units coupled to an interconnect network and reconfigurable in response to the plurality of executable information modules; and

a matrix interconnection network coupled to the plurality of reconfigurable matrices, the matrix interconnection network capable of configuring the plurality of reconfigurable matrices in response to the first executable information module for a first operating mode and to provide corresponding operand data to the plurality of reconfigurable matrices for the first operating mode, and capable of reconfiguring the plurality of reconfigurable matrices in response to the second executable information module for a second operating mode and to provide corresponding operand data to the plurality of reconfigurable matrices for the second operating mode.

100. (Once Amended) The adaptive integrated circuit of claim 99, further comprising:

a controller coupled to the plurality of reconfigurable matrices, the controller capable of providing the plurality of executable information modules to the reconfigurable matrices and to the matrix interconnection network.

102. (Once Amended) An adaptive integrated circuit, comprising:

a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

a plurality of heterogeneous computational elements, a first computational element of the plurality of heterogeneous computational elements having a first fixed architecture and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture, the first fixed architecture being different than the second fixed architecture;

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network capable of configuring the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes in response to the first configuration information, and capable of providing the first operand data to the plurality of heterogeneous computational elements for the first operating mode, and the interconnection network further capable of reconfiguring the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes in response to the second configuration information, the first functional mode being different than the second functional mode, and capable of providing the second operand data to the plurality of heterogeneous computational elements for the second operating mode;

wherein a first subset of the plurality of heterogeneous computational elements is configured for a controller operating mode, the controller operating mode comprising at least two of the following corresponding functions: directing configuration and reconfiguration of the plurality of heterogeneous computational elements, selecting the first configuration information and the second configuration information from the first executable information module, and coordinating the configuration and reconfiguration of the plurality of heterogeneous computational elements with respective first operand data and second operand data; and

wherein a second subset of the plurality of heterogeneous computational elements is configured for a memory operating mode for storing the first configuration information and the second configuration information.

103. (Once Amended) An adaptive integrated circuit, comprising:

a first executable information module, the module having first configuration information and second configuration information, the module further having first operand data and second operand data;

a plurality of heterogeneous computational elements, a first computational element of the plurality of heterogeneous computational elements having a first fixed architecture of a plurality of fixed architectures and a second computational element of the plurality of heterogeneous computational elements having a second fixed architecture of the plurality of fixed architectures, the first fixed architecture being different than the second fixed architecture, and the plurality of fixed architectures comprising at least two of the following functions: memory, addition, multiplication, complex multiplication, subtraction, configuration, reconfiguration, control, input, output, and field programmability; and

an interconnection network coupled to the plurality of heterogeneous computational elements, the interconnection network capable of configuring the plurality of heterogeneous computational elements for a first functional mode of a plurality of functional modes in response to the first configuration information, the interconnection network further capable of reconfiguring the plurality of heterogeneous computational elements for a second functional mode of the plurality of functional modes in response to the second configuration information, the first functional mode being different than the second functional mode, and the plurality of functional modes comprising at least two of the following functional modes: linear algorithmic operations, non-linear algorithmic operations, finite state machine operations, memory operations, and bit-level manipulations, and the interconnection network further capable of respectively providing first operand data and second operand data to the plurality of heterogeneous computational elements for the first functional mode and for the second functional mode.